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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/022,051	12/17/2001	Brian E. Corrigan III	01-776	2008

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EXAMINER
TORRES, JOSEPH D

ART UNIT	PAPER NUMBER
2133	4

DATE MAILED: 06/16/2004

LSI Logic Corporation
Corporate Legal Department
Intellectual Property Services Group
1551 McCarthy Boulevard, M/S D-106
Milpitas, CA 95035

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/022,051	CORRIGAN, BRIAN E.
	Examiner	Art Unit
	Joseph D. Torres	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2,3*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

> The oath or declaration is defective because:
> It does not identify the mailing address of each inventor. A mailing address is an address at which an inventor customarily receives his or her mail and may be either a home or business address. The mailing address should include the ZIP Code designation. The mailing address may be provided in an application data sheet or a supplemental oath or declaration. See 37 CFR 1.63(c) and 37 CFR 1.76.

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: '142' in Figure 1. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Kocol; James E. et al. (US 4387441 A, hereafter referred to as Kocol).

35 U.S.C. 102(b) rejection of claim 1.

Kocol teaches a method for protecting a data transfer (CRC Generate Circuit 172 in the Message Control Circuit 144 of Figure 15 provides a method for protecting a data transfer), comprising: receiving a data transfer request, wherein the data transfer request comprises a request address (col. 35, lines 9-13 in Kocol teach that a request in the form of a header only message comprising a request address at which requested data is to be stored in memory is used to initiate a transfer from a device to memory); determining whether the request address is within a generate address range (col. 36, lines 1-10 in Kocol teach that a mailbox for a subsystem is defined by a generate address range starting at a "BASE" address value and ending at a "LMIT" address value and "BASE" and "LMIT" registers are initially loaded by the corresponding subsystems; col. 36, lines 25-37 in Kocol teach that the address of each byte within the message is compared to see if the address is within a generate address range defined by the "BASE" start address value and ending at a "LMIT" end address value for the mailbox); sending generate information to a hardware computation engine (generate information includes XCRCGEN*0 in Figure 15 of Kocol, which is sent to hardware computation engine CRC Generate Circuit 172); receiving a cyclical redundancy check value from

the hardware computation engine, and storing the cyclical redundancy check value (XFIFO 174 in Figure 15 of Kocol receives cyclical redundancy check values from the hardware computation engine CRC Generate Circuit 172 and temporarily stores the cyclical redundancy check value prior to being transmitted to memory for storage).

35 U.S.C. 102(b) rejection of claim 2.

Col. 36, lines 1-10 in Kocol teach that a mailbox for a subsystem is defined by a generate address range starting at a "BASE" address value and ending at a "LMIT" address value and "BASE" and "LMIT" registers are initially loaded by the corresponding subsystems.

35 U.S.C. 102(b) rejection of claim 3.

Figure 15 in Kocol provides a hardware block diagram for an "on-the-fly" message control circuit for generating CRC during data transfers and simultaneously as part of the data transfer to memory.

35 U.S.C. 102(b) rejection of claim 4.

Figure 15 in Kocol provides a hardware block diagram for an "on-the-fly" message control circuit for generating CRC during data transfers and simultaneously as part of data transfers to memory. Note: the memory area to which data is written is protected by CRC code.

35 U.S.C. 102(b) rejection of claims 5 and 6.

CRC Generate Circuit 172 in the Message Control Circuit 144 of Figure 15 provides a method for protecting a data transfer during a write request. Note: the memory area to which data is written is protected by CRC code.

35 U.S.C. 102(b) rejection of claim 7.

Kocol teaches that determining whether the request address is within a check address range if the request address is not within a generate address range (col. 36, lines 13-47 in Kocol teach that header information is stored in mailbox 350 if or even if the request address is not within the generate address range; Note: Figure 12A teaches that the Header includes CRC check data hence the address range for mailbox 350 determined by the "BASE" and the "LMIT" address values for mailbox 350 is a check address range); sending check information to the hardware computation engine (Figure 15 is a message control circuit for all mailboxes including mailbox 350, hence check information is sent to the hardware computation engine CRC Generate Circuit 180), receiving a cyclical redundancy check result from the hardware computation engine (mailbox 350 receives the cyclical redundancy check result from the hardware computation engine CRC Generate Circuit 180 via XFIFO 174).

35 U.S.C. 102(b) rejection of claim 8.

Col. 36, lines 13-47 in Kocol teach that if the request address is not within the generate address range the message data is aborted before sending the message to the

message control circuit of Figure 15, hence the message data transfer to DMA is performed without CRC (Note also that the message header is still stored in mailbox 350).

35 U.S.C. 102(b) rejection of claim 9.

Figure 15 in Kocol provides a hardware block diagram for an "on-the-fly" message control circuit for generating CRC during data transfers and simultaneously as part of data transfers to memory. Note: the memory area to which data is written is protected by CRC code.

35 U.S.C. 102(b) rejection of claim 10.

Col. 20, lines 56-68 in Kocol teach that generate information provided to the message control circuit of Figure 15 includes destination or request address information.

35 U.S.C. 102(b) rejection of claim 11.

Kocol teaches a method for protecting a data transfer (CRC Generate Circuit 172 in the Message Control Circuit 144 of Figure 15 provides a method for protecting a data transfer), comprising: receiving a data transfer request, wherein the data transfer request comprises a request address (col. 35, lines 9-13 in Kocol teach that a request in the form of a header only message comprising a request address at which requested data is to be stored in memory is used to initiate a transfer from a device to memory); determining whether the request address is within a check address range (col. 36, lines

1-10 in Kocol teach that a mailbox for a subsystem is defined by a generate address range starting at a "BASE" address value and ending at a "LMIT" address value and "BASE" and "LMIT" registers are initially loaded by the corresponding subsystems; col. 36, lines 25-37 in Kocol teach that the address of each byte within the message is compared to see if the address is within an address range defined by the "BASE" start address value and ending at a "LMIT" end address value for the mailbox; Note: Figure 12A teaches that the Header includes CRC check data hence the address range for mailbox 350 determined by the "BASE" and the "LMIT" address values for mailbox 350 is a check address range); sending check information to a hardware computation engine (col. 36, lines 13-47 in Kocol teach that header information is stored in mailbox 350 if or even if the request address is not within the generate address range; Note: Figure 12A teaches that the Header includes CRC check data hence the address range for mailbox 350 determined by the "BASE" and the "LMIT" address values for mailbox 350 is a check address range; Figure 15 is a message control circuit for all mailboxes including mailbox 350, hence check information is sent to the hardware computation engine CRC Generate Circuit 180); and receiving a cyclical redundancy check result from the hardware computation engine (mailbox 350 receives the cyclical redundancy check result from the hardware computation engine CRC Generate Circuit 180 via XFIFO 174).

35 U.S.C. 102(b) rejection of claim 12.

Col. 36, lines 1-10 in Kocol teach that mailbox 350 for a subsystem is defined by a generate address range starting at a "BASE" address value and ending at a "LMIT" address value and "BASE" and "LMIT" registers are initially loaded by the corresponding subsystems.

35 U.S.C. 102(b) rejection of claim 13.

Col. 19, lines 1-5 teach that a CRC check is performed on data received from the system bus during data transfer.

35 U.S.C. 102(b) rejection of claim 14.

CRC is error correction information.

35 U.S.C. 102(b) rejection of claim 15.

XFIFO 174 in Figure 15 of Kocol receives cyclical redundancy check values from the hardware computation engine CRC Generate Circuit 172 and temporarily stores the cyclical redundancy check value prior to being transmitted to memory for storage.

35 U.S.C. 102(b) rejection of claim 16.

Figure 15 in Kocol provides a hardware block diagram for an "on-the-fly" message control circuit for generating CRC during data transfers and simultaneously as part of data transfers to memory. Note: the memory area to which data is written is protected by CRC code.

35 U.S.C. 102(b) rejection of claims 17-20.

CRC Generate Circuit 172 in the Message Control Circuit 144 of Figure 15 in Kocol provides a method for protecting a data transfer during a read and write requests. Note: the memory area to which data is written is protected by CRC code.

35 U.S.C. 102(b) rejection of claim 21.

Kocol teaches an apparatus for protecting a data transfer (CRC Generate Circuit 172 in the Message Control Circuit 144 of Figure 15 in Kocol provides a method for protecting a data transfer), comprising: a memory interface logic (DMA Controller 140 in Figures 14 and 23 is memory interface logic); a system memory coupled to the memory interface logic (A Controller 140 in Figures 14 and 23 is coupled to system memory); a hardware computation engine (Message Control Circuit 144 of Figure 15 in Kocol is a hardware computation engine), wherein the hardware computation engine is coupled to the memory interface logic by a memory monitor bus and a memory read/write bus (the hardware computation engine Message Control Circuit 144 of Figure 15 in Kocol is coupled to the memory interface logic MA Controller 140 in Figures 14 and 23 by a memory monitor bus and a memory read/write bus), wherein the memory interface logic receives a data transfer request, wherein the data transfer request comprises a request address, determines whether the request address is within a generate address range (col. 35, lines 9-13 in Kocol teach that a request in the form of a header only message comprising a request address at which requested data is to be stored in memory is used

to initiate a transfer from a device to memory); sends generate information to a hardware computation engine via the memory monitor bus (generate information includes XCRCGEN*0 in Figure 15 of Kocol, which is sent to hardware computation engine CRC Generate Circuit 172); receives a cyclical redundancy check value from the hardware computation engine via the memory read/write bus; and stores the cyclical redundancy check value in the system memory (XFIFO 174 in Figure 15 of Kocol receives cyclical redundancy check values from the hardware computation engine CRC Generate Circuit 172 and temporarily stores the cyclical redundancy check value prior to being transmitted to memory for storage).

35 U.S.C. 102(b) rejection of claim 22.

Col. 36, lines 1-10 in Kocol teach that a mailbox for a subsystem is defined by a generate address range starting at a "BASE" address value and ending at a "LMIT" address value and "BASE" and "LMIT" registers are initially loaded by the corresponding subsystems.

35 U.S.C. 102(b) rejection of claim 23.

Figure 15 in Kocol provides a hardware block diagram for an "on-the-fly" message control circuit for generating CRC during data transfers and simultaneously as part of the data transfer to memory.

35 U.S.C. 102(b) rejection of claim 24.

Figure 15 in Kocol provides a hardware block diagram for an "on-the-fly" message control circuit for generating CRC during data transfers and simultaneously as part of data transfers to memory. Note: the memory area to which data is written is protected by CRC code.

35 U.S.C. 102(b) rejection of claim 25.

Kocol teaches an apparatus for protecting a data transfer (CRC Generate Circuit 172 in the Message Control Circuit 144 of Figure 15 in Kocol provides a method for protecting a data transfer), comprising: a memory interface logic (DMA Controller 140 in Figures 14 and 23 is memory interface logic); a system memory coupled to the memory interface logic (A Controller 140 in Figures 14 and 23 is coupled to system memory); a hardware computation engine (Message Control Circuit 144 of Figure 15 in Kocol is a hardware computation engine), wherein the hardware computation engine is coupled to the memory interface logic by a memory monitor bus and a memory read/write bus (the hardware computation engine Message Control Circuit 144 of Figure 15 in Kocol is coupled to the memory interface logic MA Controller 140 in Figures 14 and 23 by a memory monitor bus and a memory read/write bus), wherein the memory interface logic receives a data transfer request, wherein the data transfer request comprises a request address (col. 35, lines 9-13 in Kocol teach that a request in the form of a header only message comprising a request address at which requested data is to be stored in memory is used to initiate a transfer from a device to memory); determining whether the request address is within a check address range (col. 36, lines 1-10 in Kocol teach that

a mailbox for a subsystem is defined by a generate address range starting at a "BASE" address value and ending at a "LMIT" address value and "BASE" and "LMIT" registers are initially loaded by the corresponding subsystems; col. 36, lines 25-37 in Kocol teach that the address of each byte within the message is compared to see if the address is within an address range defined by the "BASE" start address value and ending at a "LMIT" end address value for the mailbox; Note: Figure 12A teaches that the Header includes CRC check data hence the address range for mailbox 350 determined by the "BASE" and the "LMIT" address values for mailbox 350 is a check address range); sends check information to a hardware computation engine via the memory monitor bus (col. 36, lines 13-47 in Kocol teach that header information is stored in mailbox 350 if or even if the request address is not within the generate address range; Note: Figure 12A teaches that the Header includes CRC check data hence the address range for mailbox 350 determined by the "BASE" and the "LMIT" address values for mailbox 350 is a check address range; Figure 15 is a message control circuit for all mailboxes including mailbox 350, hence check information is sent to the hardware computation engine CRC Generate Circuit 180); and receives a cyclical redundancy check result from the hardware computation engine via the memory read/write bus (mailbox 350 receives the cyclical redundancy check result from the hardware computation engine CRC Generate Circuit 180 via XFIFO 174).

35 U.S.C. 102(b) rejection of claim 26.

Col. 36, lines 1-10 in Kocol teach that mailbox 350 for a subsystem is defined by a generate address range starting at a "BASE" address value and ending at a "LMIT" address value and "BASE" and "LMIT" registers are initially loaded by the corresponding subsystems.

35 U.S.C. 102(b) rejection of claim 27.

Col. 19, lines 1-5 teach that a CRC check is performed on data received from the system bus during data transfer.

35 U.S.C. 102(b) rejection of claim 28.

CRC is error correction information.

35 U.S.C. 102(b) rejection of claim 29.

XFIFO 174 in Figure 15 of Kocol receives cyclical redundancy check values from the hardware computation engine CRC Generate Circuit 172 and temporarily stores the cyclical redundancy check value prior to being transmitted to memory for storage.

35 U.S.C. 102(b) rejection of claim 30.

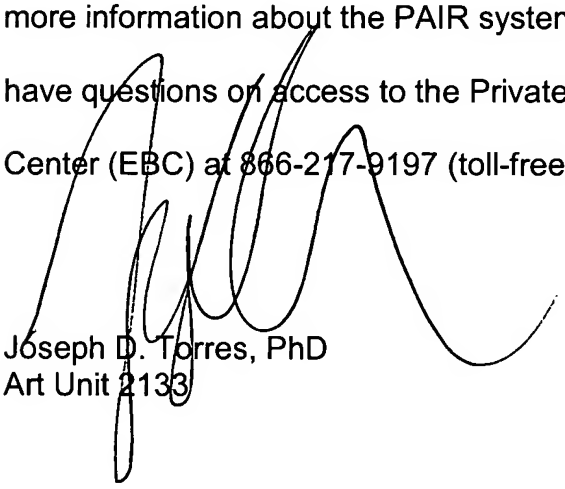
Figure 15 in Kocol provides a hardware block diagram for an "on-the-fly" message control circuit for generating CRC during data transfers and simultaneously as part of data transfers to memory. Note: the memory area to which data is written is protected by CRC code.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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